EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	212	(memory and (floating adj gate) and (control adj gate) and drain and source and electrons and (non adj volatile)).clm.	US-PGPUB; USPAT	OR	ON	2006/06/06 14:20
L2	78	1 and @ad<"19981110"	US-PGPUB; USPAT	OR	ON	2006/06/06 14:20
L3	768	438/257,262-264.ccls. and @ad<"19981110"	US-PGPUB; USPAT	OR	ON	2006/06/06 14:31
L4	599	3 and (floating adj gate) and (control adj gate) and drain and source	US-PGPUB; USPAT	OR	ON	2006/06/06 14:31
L5	452	4 and electrons	US-PGPUB; USPAT	OR	ON	2006/06/06 14:31
L6	776	257/315,320,322.ccls. and @ad<"19981110"	US-PGPUB; USPAT	OR	ON	2006/06/06 14:31
L7	614	6 and (floating adj gate) and (control adj gate) and drain and source	US-PGPUB; USPAT	OR	ON	2006/06/06 14:31
L8	530	7 and electrons	US-PGPUB; USPAT	OR	ON	2006/06/06 14:31
L9	479	8 not 5	US-PGPUB; USPAT	OR	ON	2006/06/06 14:31

US-PAT-NO: 6124157

DOCUMENT-IDENTIFIER: US 6124157 A

TITLE: Integrated non-volatile and random access memory and method of forming the same

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Detailed Description Text - DETX (16):

During a programming operation, the drain junction depletion region is generally kept in a weak junction avalanche state to supply **electrons to the floating gate** 112. As a result, the programming current may be less than 1 nA when the control gate voltage is either about 5 volts or 9 volts. The low programming current may be achieved due to higher **electron** injection efficiency (and thus lower programming power consumption) and less heat generation during programming may result. A programming time of

Detailed Description Text - DETX (18):

The memory cell 18 may be erased by Fowler-Nordheim tunneling specifically, or grounding the memory cell source and the gate, source or drain of the select transistor 108 and applying a negative voltage of between approximately -5 to -20 volts, preferably -8 to -12 volts, to the control gate 110 and applying a positive voltage of between approximately 0 to 5 volts, preferably 4 to 5 volts, to the cell drain 122. One suitable voltage combination for erasing the memory cell 18 is to apply -10 volts on the control gate 110 and +5 volts on the cell drain 122, all other cell electrodes being grounded. A high electric field may be created across the tunnel oxide by the voltages on the drain of the storage transistor 106 and the control gate. As a result, **electrons** may be tunneling from the control gate to the drain of the storage transistor 106. The source of the storage transistor 106 may be electrically floating as a result of grounding the select transistor 108.